REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Disclosure Objections

The Examiner objected to the disclosure because the title of the invention appears to improperly use the work "observer." The title has been changed to "ON-CHIP OBSERVABILITY BUFFER TO OBSERVE BUS TRAFFIC."

35 U.S.C. § 112 Rejections

Examiner rejected claims 1-18 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Corrections have been made with the foregoing amendments.

Prior Art Rejections

Examiner rejected claims 1, 6, 10 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,488,688 (hereinafter "Gonzales"). Examiner rejected claims 1, 6, 10 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,903,719 (hereinafter "Yamamoto"). Examiner rejected claims 1, 6, 10 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,119,254 (hereinafter "Assouad"). Examiner rejected claims 1, 2, 6, 7, 10, 11, 14 and 15 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,072,804 (hereinafter "Beyers")

in view of U.S. Patent 5,933,594 (hereinafter "La Joie"). Gonzales, Yamamoto, Assoud, Beyers, and La Joie, are hereinafter collectively "References."

Applicant's independent claims 1, 6, 10 and 14 of the present application include limitations not disclosed or taught by the References. As a result, claims 1, 6, 10 and 14 are not anticipated and are patentable over the referneces.

In particular, applicant's claims, as amended, include the limitation, or a limitation similar there to, of:

> a buffer having at least one trigger, integrated on a component connected with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to observe and echo a predetermined finite set of bi-direction signals transmitted on said memory bus. . . (emphasis added) (Applicant's claim 1 as amended).

The References, however, do not disclose nor suggest the limitations as claimed by applicant. The Reference do not disclose the claimed limitation of a buffer connected with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to observe and echo a predetermined finite set of bi-direction signals transmitted on said memory bus.

Therefore, in view of applicant's independent claims including limitations that are not disclosed nor suggested by the references, applicant's independent claims are not anticipated and are patentable over the References.

In addition, the remaining claims depend from one of the independent claims as discussed above, and therefore include similar limitations, and as a result are also patentable over the References.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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John P. Ward
Reg. No. 40,216

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300